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IN THE CLAIMS

Please cancel claims 1-8, 16-17 and 19-20.

Please amend the claims as follows.

1-8 (Cancelled)

9. (Currently amended) An integrated circuit comprising:

a register file bit comprising:

a primary latch having a data input and a data output;

a plurality of secondary latches each having a data input and a data output;

a feedback path from the data ~~output~~ outputs of the plurality of secondary latches to the data input of the ~~first~~ primary latch, the feedback path including a data selection mechanism for selecting any one data output from the plurality of secondary latches to feed back to the data input of the ~~first~~ primary latch; and

a context switch mechanism for switching data between the primary latch and each of the plurality of secondary latches that causes the data on the data output of the primary latch to be written to a selected one of the plurality of secondary latches, and that causes the data on the data output of the selected one secondary latch to be written to the primary latch.

10. (Original) The integrated circuit of claim 9 wherein the context switch mechanism comprises a swap signal coupled to the primary latch.

11. (Original) The integrated circuit of claim 9 wherein the context switch mechanism comprises a delay element between the data output of the primary latch and the data inputs of the plurality of secondary latches.